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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,291	04/08/2004	Gurtej Sandhu Sandhu	303.085US7	8616

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EXAMINER	
LE, DUNG ANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,291	SANDHU ET AL.	
	Examiner	Art Unit	
	DUNG A. LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on 7/31/06

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-14* is/are pending in the application.

4a) Of the above claim(s) *1-9 and 25-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/26/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DLe

Continuation data:

This application is a Divisional of U.S. Application No. 10/217,620, filed August 13, 2002, which is a Divisional of U.S. Application No. 09/652,619, filed August 31, 2000, which is a Continuation of U.S. Application No. 08/912,051, filed August 18, 1997, now U.S. Patent No. 6,144,095, which is a Continuation of U.S. Application No. 08/656,712, filed June 3, 1996, now U.S. Patent No. 5,662,788.

Oath/Declaration

The oath/declaration filed on 4/8/2004is acceptable.

Election/Restriction

Application's election traverse of Species II: 10-24 is acknowledged for prosecution in the subject application .

Information Disclosure Statement

This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 4/8/2004 and 4/26/2006 has/have been considered and made of record. The references cited on the PTOL 1449 form have been considered.

Specification

The specification is objected to for the following reason:

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

In **Claim 14 and 15**, limitations "a third voltage" and a fourth voltage" are not support in Specification.

In **Independent claims 10 and 14**, limitations "retain metal ions on the exposed ..." are not support in Specification.

In **Independent claim 20**, limitation "retain copper ions on the exposed ..." is not support in Specification.

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

a) Claims 10,14-15 and 20 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the

specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant introduces the new matter by adding :

"a third voltage" and " a fourth voltage" in to **Claim 14 and 15;** "retain metal ions on the exposed ..." into **Independent claims 10 and 14,** "retain copper ions on the exposed ..." into **Independent claim 20.**

The added matter(s) is(are) not supported in the Specification and it (they) (is) are not satisfactory resolved and consequently raise doubt as to possession o the claimed invention at the time of filling.

b) The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Set of Claims 10-15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of Patent 6171952 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because *it would have been obvious to one of ordinary skill in the art at the time of the invention was made to* form the steps of placing the semiconductor device in an electrolytic bath; applying a first voltage between the substrate and an anode, the first voltage being sufficient to deposit metal ions on the exposed first layer and the exposed second layer; and applying a second voltage between the substrate and the anode, the second voltage being sufficient to remove metal ions from the exposed first layer and retain metal ions on the exposed second layer *by* introducing the steps of producing a first surface potential on the first layer and a second surface potential on the second layer, wherein the second surface potential is higher

than the first surface potential; applying a first voltage between the substrate and an anode in the presence of an electrolytic bath containing metal ions, wherein a potential difference between the first voltage and the first surface potential exceeds a reduction potential of the metal, thereby depositing the metal on the exposed portion of the first layer and the remaining portion of the second layer; and

applying a second voltage between the substrate and the anode in the presence of the electrolytic bath containing the metal ions, wherein a potential difference between the second voltage and the first surface potential is less than a reverse deposition potential of the metal, thereby removing the metal from the exposed portion of the first layer *in order to* define inventive Method for depositing metal on a semiconductor device having a substrate, an exposed first surface and an exposed second surface.

Set of claims 16-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **claim 9 of Patent 5,662,788.** Although the conflicting claims are not identical, they are not patentably distinct from each other because *it would have been obvious to one of ordinary skill in the art at the time of the invention was made to* form the steps of placing the semiconductor substrate with the first and second layers in an electrolytic bath comprising a solution of metal ions; applying a bi-polar modulated voltage having a positive duty cycle and a negative duty cycle to the electrolytic bath, the voltage and

surface potentials selected such that the metal is deposited on the remaining portions of the second layer and that metal deposited on the first layer during a positive duty cycle is removed from the first layer during a negative duty cycle; and selectively removing exposed portions of the first layer *by* placing the first and second layers at different surface potentialselectro-depositing the first and second layers in a solution of metal ions by applying a bi-polar modulated voltage having a positive duty cycle and a negative duty cycle, the voltage and surface potentials selected such that the metal is deposited on the remaining portions of the second layer and that metal deposited on the first layer during a positive duty cycle is removed from the first layer during a negative duty cycle; and selectively removing exposed portions of the first layer *in order to* define inventive Method for depositing metal on a semiconductor device having a substrate, an exposed first surface and an exposed second surface.

Set of claims 21-24 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **claims 9 and 11 of Patent 5,662,788.** Although the conflicting claims are not identical, they are not patentably distinct from each other because *it would have been obvious to one of ordinary skill in the art at the time of the invention was made to* form the steps of placing the semiconductor substrate with the first and second layers in an electrolytic bath comprising a solution of metal ions; applying a bi-polar modulated voltage having a positive duty cycle and a negative duty cycle to the electrolytic bath, the voltage and

surface potentials selected such that the metal is deposited on the remaining portions of the second layer and that metal deposited on the first layer during a positive duty cycle is removed from the first layer during a negative duty cycle; and selectively removing exposed portions of the first layer, wherein the step of placing the semiconductor substrate with the first and second layers in an electrolytic bath comprises the step of placing the semiconductor substrate with the first and second layers in an electrolytic bath containing copper ions in solution *by* placing the first and second layers at different surface potentials electro-depositing the first and second layers in a solution of metal ions by applying a bi-polar modulated voltage having a positive duty cycle and a negative duty cycle, the voltage and surface potentials selected such that the metal is deposited on the remaining portions of the second layer and that metal deposited on the first layer during a positive duty cycle is removed from the first layer during a negative duty cycle; and selectively removing exposed portions of the first layer *in order to* define inventive Method for depositing copper on a semiconductor device having a substrate, an exposed first surface and an exposed second surface.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, M. Smith can be reached on (571) 272-1907. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818